What is claimed is:

1. A device for controlling a frequency response comprising:

a filter, wherein the filter generates an output signal after removing a frequency from an input signal; and

a duty ratio controller, wherein the duty ratio controller controls a duty ratio of a clock signal, and generates a duty-controlled clock signal.

2. The device of claim 1, wherein the filter further comprises:

a first impedance component; and

a switch that is serially connected to the first impedance component, wherein the switch is switched on or off in response to the duty-controlled clock signal.

3. The device of claim 1, wherein the duty ratio controller further comprises:

a flip-flop, wherein the flip flop receives a delayed signal after obtaining the clock signal by a time delay.

4. The device of claim 3, wherein the duty ratio controller further comprises:

a delay component, wherein the delay component receives the clock signal, generates the delayed signal, and controls the time delay in response to a duty control signal.

5. The device of claim 1, wherein the first impedance component and the switch are serially connected between an output node and a voltage node of the filter.

6. The device of claim 1, wherein the filter further comprises:

a second impedance component, that is connected to an input node and an output node of the filter.

7. The device of claim 1, wherein the filter further comprises:

an amplifier;

a second impedance component that is connected to one terminal of the amplifier and an output node of the filter; and

a third impedance component that is connected to the one terminal of the

amplifier and an input node of the filter, wherein the first impedance component and the switch are serially connected between one terminal of the amplifier and the output node of the filter.

8. The device of claim 7, wherein the first impedance component is a capacitor, and the second and third impedance components are resistors.

9. The device of claim 7, wherein the first and third impedance components are resistors, and the second impedance component is a capacitor.

10. The device of claim 1, wherein the duty ratio of the duty-controlled clock signal is controlled in response to the duty control signal.

11. The device of claim 1, wherein the switch is a MOS transistor.

12. The device of claim 1, wherein the switch is positioned in a transmission path.

13. The device of claim 1, wherein the switch is positioned on a transmission path between an input node and an output node of the device when another transmission path exists between an input node and an output node of the device.

14. The device of clam 1, wherein the output signal is generated after removing the frequency at a predetermined band from the input signal.

15. A device for controlling a frequency response comprising:

a filter, wherein the filter generates an output signal after removing a frequency from an input signal, wherein a frequency response of the filter varies in response to a duty ratio of a duty-controlled clock signal; and

a duty ratio controller, wherein the duty ratio controller generates the duty-controlled clock signal.

16. The device of claim 15, wherein the filter further comprises:

an impedance component; and

a switch that is serially connected to the impedance component, wherein the switch is switched on or off by the duty-controlled clock signal.

17. The device of claim 15, wherein the duty ratio controller receives a clock signal and generates the duty-controlled clock signal in response to a duty control signal.

18. The device of claim 15, wherein the switch is positioned on a transmission path.

19. The device of claim 15, wherein the switch is positioned on a transmission path between an input node and an output node of the device when another transmission path exists between an input node and an output node of the device.

20. The device of claim 15, wherein the output signal is generated after removing the frequency at a predetermined band from the input signal.